Conversion from Xilinx® to Atmel® FPGAs

Xilinx Conversion

Application Note

Atmel's AT40K family is pin compatible with the Xilinx 4000, 5200 and Spartan® families. Atmel's IDS software can convert XNF designs from Xilinx 3000, 4000 and 5200 families. Atmel can also accept a number of other design formats with varying degrees of effort required for each.

Part Capacity

For 5200 family conversions, the part number for the 5200 and AT40K families are usually similar.

For the Xilinx 4000 family there are a number of architecture-specific features which can increase the size of the design in an Atmel part.

If a Xilinx XC4000 design uses RAM, then the size of the design will decrease in an Atmel part as we do not sacrifice logic to implement the RAM. If an XC4000 design contains clock enables on FFs, this can increase the design size.

The following tables therefore give only a rough indication of the equivalent part for the 4000 family as each design will be different.

Table 1 shows the resources available in each Atmel device. The following tables show the comparison of resources.

Table 1. Atmel AT40K FPGAs

Family	Gate Range	Block Array	RAM Bits	Register	Typical RAM Bits	I/O
AT40K05	5K-10K	16 x 16	2,048	256	2,048	128
AT40K10	10K-20K	24 x 24	4,608	576	4,608	192
AT40K20	20K-30K	32 x 32	8,192	1,024	8,192	256
AT40K40	40K-50K	48 x 48	18,432	2,304	18,432	384

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Table 2. Xilinx 4000 FPGAs

Family	Gate Range	Block Array	RAM Bits	Reg.	Typical RAM Bits	I/O	Equiv. Atmel Family	Reg.	RAM Bits
XC4002	1K-3K	8 x 8	2,048	256		64	AT40K05	256	2,048
XC4003	2K-5K	10 x 10	3,200	360	960	80	AT40K05/10	256/576	2,048/4,096
XC4005	3K-9K	14 x 14	6,272	616	1,882	112	AT40K10/20	576/1,024	4,608/8,192
XC4006	4K-12K	16 x 16	8,192	768	2,458	128	AT40K10/20	576/1,024	4,608/8,192
XC4008	6K-15K	18 x 18	10,368	936	3,110	144	AT40K10/20	576/1,024	4,608/8,192
XC4010	7K-20K	20 x 20	12,800	1,120	3,840	160	AT40K10/20	576/1,024	4,608/8,192
XC4013	10K-30K	24 x 24	18,432	1,536	5,330	192	AT40K20/40	1,024/2,304	8,192/18,432
XC4020	13K-30K	28 x 28	25,088	2,016	7,526	224	AT40K20/40	1,024/2,304	8,192/18,432
XC4025	15K-45K	32 x 32	32,768	2,560	9,830	256	AT40K40	2,304	18,432
XC4028	18K-50K	32 x 32	32,768	2,560	9,830	256	AT40K40	2,304	18,432
XC4036	22K-65K	36 x 36	41,472	3,168	12,442	288	AT40K40	2,304	18,432

Table 3. Xilinx 5200 FPGAs

Family	Gate Range	Block Array	RAM Bits	Reg.	Typical RAM Bits	I/O	Equiv. Atmel Family	Reg.	RAM Bits
XC5202	2K-3K	8 x 8	None	256	None	84	AT40K05	256	2,048
XC5204	4K-6K	10 x 12	None	480	None	124	AT40K05/10	256/576	2,048/4,096
XC5206	6K-10K	14 x 14	None	784	None	148	AT40K10/20	576/1,024	4,608/8,192
XC5210	10K-16K	18 x 18	None	1,296	None	196	AT40K10/20	576/1,024	4,608/8,192
XC5215	15K-23K	22 x 22	None	1,936	None	244	AT40K20/40	1,024/2,304	8,192/18,432

Table 4. Spartan FPGAs

Family	Gate Range	Block Array	RAM Bits	Reg.	Typical RAM Bits	I/O	Equiv. Atmel Family	Reg.	RAM Bits
XCS05	2K-5K	10 x 10	3,200	360	960	77	AT40K05/10	256/576	2,048/4,096
XCS10	3K-10K	14 x 14	6,272	616	1,882	112	AT40K10/20	576/1,024	4,608/8,192
XCS20	7K-20K	20 x 20	12,800	1,120	3,840	160	AT40K20/40	1,024/2,304	8,102/18,432
XCS30	10K-30K	24 x 24	18,432	1,536	5,530	192	AT40K40	2,304	18,432
XCS40	13K-40K	28 x 28	25,088	2,016	7,526	205	AT40K40	2,304	18,432

Pin Compatibility and Device Configuration

Atmel parts are pin-compatible with the Xilinx 4000, 5200 and Spartan families. The following limitations to this apply.

JTAG - Designs requiring JTAG are not recommended as Xilinx implements this differently;

Mode Pins - Mode pins M0, M1 and M2 cannot be used as User I/O in Atmel parts; and

Configuration Modes - Designs using Configuration Mode 0 or Mode 7 are ideal for drop-in replacement of the Xilinx part. Other configuration modes would require further investigation and you should request factory assistance for doing this.

CON Pin - On 5200 device it is not necessary to drive the CON pin low to initialize configuration. For the Atmel part it is necessary to drive the CON pin low for three clock cycles; required for Mode 7 and 1.

The AT40K family does not require the pin O, TDO as Xilinx does. Xilinx uses this for JTAG support. Atmel provides an extra user IO in its place.

The GCLK pins in the Atmel and Xilinx devices are all in the same location, the only difference is the names. This is shown in the tables.

The Spartan family's 208-lead and 240-lead PQFPs are not pin compatible with the Xilinx 4000 and 5200 families. In turn, Spartan FPGAs in the 208-lead and 240-lead PQFP packages are also not pin compatible with the AT40K.

The following tables show the differences in pinout between the Atmel and Xilinx devices.

Table 5. Atmel vs Xilinx FPGAs Pinout Table - XC4000

Family	Package				Equiv. Atmel Family	Package			
XC4002	**PC84**	**VQ100**			**AT40K05**	**PC84**	**VQ100**		
O, TDO	P.75	P.76			I/O104	P.75	P.76		
XC4003	**PC84**	**VQ100**			**AT40K05**	**PC84**	**VQ100**		
I/O, PGCK2	P.35	P.27			I/O33, GCK3	P.35	P.27		
I/O, SGCK3	P.51	P.48			I/O64, GCK4	P.51	P.48		
I/O, PGCK3	P.57	P.54			I/O66, GCK5	P.57	P.54		
I/O, SGCK4 (DOUT)	P.72	P.73			I/O96, GCK6, $\overline{\text{CSOUT}}$	P.72	P.73		
XC4005	**PC84**	**PQ160**	**PQ208**		**AT40K05**	**PC84**	**PQ160**	**PQ208**	
O, TDO	P.75	P.121	P.159		I/O104	P.75	None	None	
XC4006	**PC84**	**TQ144**	**PQ160**	**PQ208**	**AT40K05**	**PC84**	**TQ144**	**PQ160**	**PQ208**
I/O, SGCK1 (A15)	P.10	P.143	P.159	P.204	I/O128, GCK8 (A15)	P.10	P.143	P.159	P.204
I/O, PGCK2	P.35	P.39	P.43	P.57	I/O33, GCK3	P.35	P.39	P.43	P.57
I/O, SGCK3	P.51	P.70	P.78	P.100	I/O64, GCK4	P.51	P.70	P.78	P.100
I/O, PGCK3	P.57	P.76	P.84	P.110	I/O66, GCK5	P.57	P.76	P.84	P.110
I/O, SGCK4 (DOUT)	P.72	P.106	P.118	P.152	I/O96, GCK6 ($\overline{\text{CSOUT}}$)	P.72	P.106	P.118	P.152
O, TDO	P.75	P.109	P.121	P.159	I/O104	P.75	P.109	None	None
I/O, PGCK4 (A1)	P.78	P.112	P.124	P.162	I/O98, GCK7 (A1)	P.78	P.112	P.124	P.162
XC4008	**PC84**	**PQ160**	**PQ208**		**AT40K05 Pad Names**	**PC84**	**PQ160**	**PQ208**	
I/O,SGCK1 (A15)	P.10	P.159	P.204		I/O192, GCK8 (A15)	P.10	P.159	P.204	
I/O, PGCK2	P.35	P.43	P.57		I/O49, GCK3	P.35	P.43	P.57	
I/O, SGCK3	P.51	P.78	P.100		I/O96, GCK4	P.51	P.78	P.100	

Table 5. Atmel vs Xilinx FPGAs Pinout Table - XC4000 (Continued)

Family	Package				Equiv. Atmel Family	Package			
I/O, PGCK3	P.57	P.84	P.110		I/O98, GCK5	P.57	P.84	P.110	
I/O, SGCK4 (DOUT)	P.72	P.118	P.152		I/O144, GCK6 ($\overline{\text{CSOUT}}$)	P.72	P.118	P.152	
O, TDO	P.75	P.121	P.159		I/O151	P.75	P.121	P.159	
I/O, PGCK4 (A1)	P.78	P.124	P.162		I/O146, GCK7 (A1)	P.78	P.124	P.162	

Table 6. Atmel vs Xilinx FPGAs Pinout Table - XCS200

Family	Package					Equiv. Atmel Family	Package				
XC5202	**PC84**	**VQ100**	**TQ144**			**AT40K05**	**PC84**	**VQ100**	**TQ144**		
GCK2 (I/O)	P.35	P.27	P.39			I/O33 GCK3	P.35	P.27	P.39		
GCK3 (I/O)	P.57	P.54	P.76			I/O66 GCK5	P.57	P.54	P.76		
GCK4 (A1, I/O)	P.78	P.79	P.112			I/O98 GCK7	A1	P.78	P.79	P.112	
XC5204	**PC84**	**VQ100**	**TQ144**	**PQ160**		**AT40K05**	**PC84**	**VQ100**	**TQ144**	**PQ160**	
GCK2 (I/O)	P.35	P.27	P.39	P.43		I/O33 GCK3	P.35	P.27	P.39	P.43	
GCK3 (I/O)	P.57	P.54	P.76	P.84		I/O66 GCK5	P.57	P.54	P.76	P.84	
GCK4 (A1, I/O)	P.78	P.79	P.112	P.124		I/O98 GCK7 A1	P.78	P.79	P.112	P.124	
XC5206	**PC84**	**VQ100**	**TQ144**	**PQ160**	**PQ208**	**AT40K10**	**PC84**	**VQ100**	**TQ144**	**PQ160**	**PQ208**
GCK2 (I/O)	P.35	P.27	P.39	P.43	P.57	I/O49 GCK3	P.35	P.27	P.39	P.43	P.57
GCK3 (I/O)	P.57	P.54	P.76	P.84	P.110	I/O98 GCK5	P.57	P.54	P.76	P.84	P.110
GCK4 (A1, I/O)	P.78	P.79	P.112	P.124	P.162	I/O146 GCK7 (A1)	P.78	P.79	P.112	P.124	P.162

Table 7. Atmel vs Xilinx FPGAs Pinout Table - Spartan

Family	Package			Equiv. Atmel Family	Package		
XCS05	**PC84**	**VQ100**		**AT40K05**	**PC84**	**VQ100**	
O, TDO	P.75	P.76		I/O104	P.75	P.76	
XCS10	**PC84**	**VQ100**	**TQ144**	**AT40K10**	**VQ100**	**TQ144**	
O, TDO	P.75	P.76	P.109	I/O151	P.76	P.109	
XCS20	**VQ100**	**TQ144**	**PQ208**	**AT40K20**	**VQ100**	**TQ144**	**PQ208**
O, TDO	P.76	P.109	P.157	I/O151	P.76	P.109	P.157
XCS30	**VQ100**	**TQ144**		**AT40K40**	**VQ100**	**TQ144**	
O, TDO	P.76	P.109		I/O301	P.76	P.109	

Replacing Xilinx Serial PROMs with the AT17 Series Configuration EEPROMs

The Xilinx serial PROM devices should be replaced by Atmel AT17 Series Configuration EEPROMs. If you replace the Xilinx FPGA, you also need to replace the Configurator. It is important to check that a compatible Atmel device is available to replace the Xilinx Configurator, especially on 8-pin DIP.

Atmel does support most of the Xilinx Configurator packages. Atmel is also currently performing a die shrink of the parts to allow us to support the rest of the Xilinx packages.

Please check with Factory Support for availability of the device you need, if it has not already been released.

Design Format

Atmel can convert designs from Xilinx using several methods.

Designs that Do Not Contain RAM

The preferred route for conversion is using VHDL or Verilog source code. It is also possible to convert designs from XNF using Atmel's IDS software or EDIF file format using Exemplar's software.

Designs Containing RAM

Some editing of the design source is required for conversion of designs containing RAM. This is because we have to replace the Xilinx specific code for Xilinx RAM with Atmel's implementation of RAM. See application notes for details, Replacing Xilinx RAM.

Schematic Designs

Atmel can also convert designs done in Viewlogic and OrCAD, but this is labor intensive and is normally carried out at the factory. This method is not recommended.

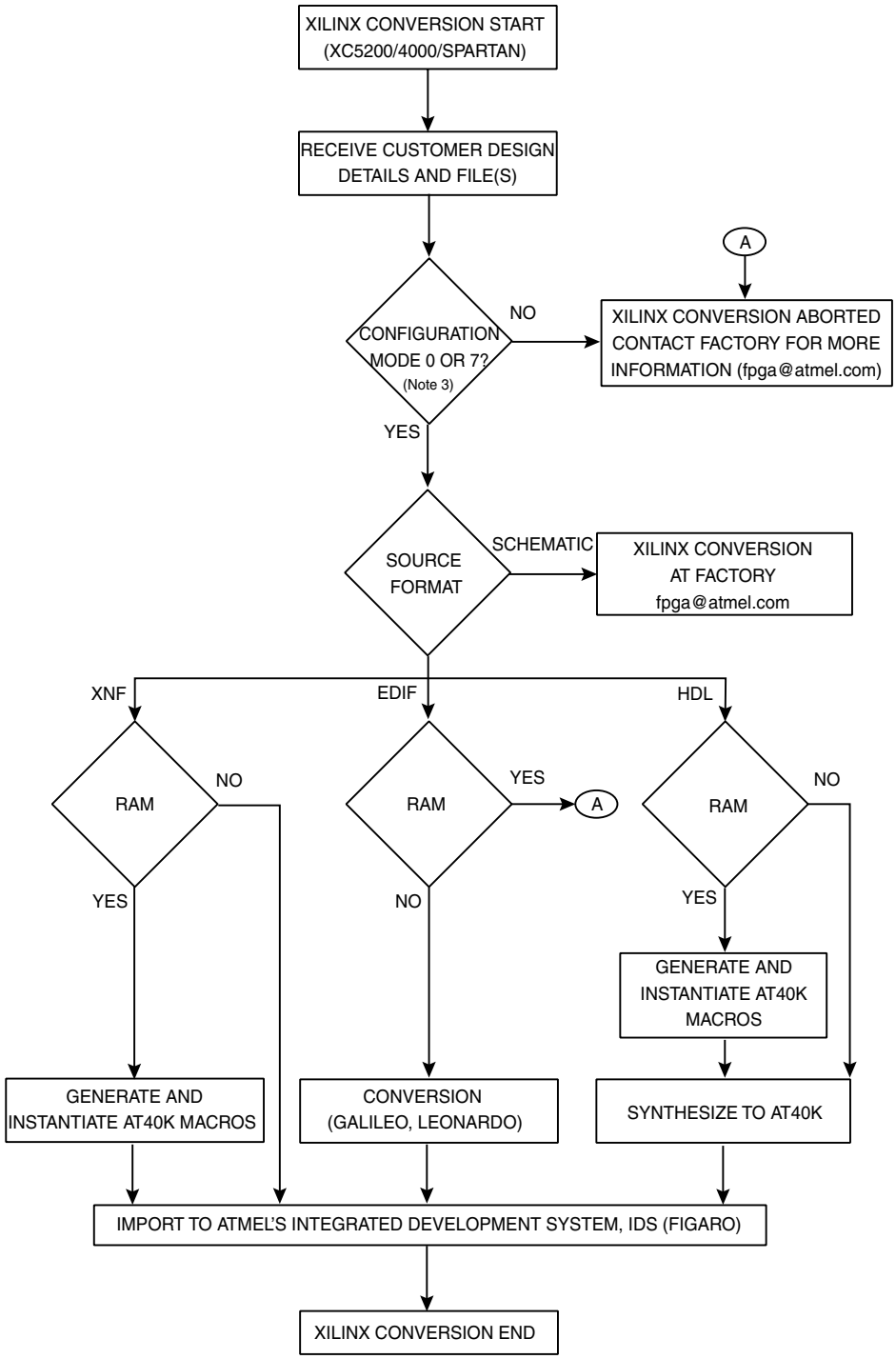
The following table lists opportunities, in descending order, by ease of conversion.

5200	4000/Spartan	Mode	Source	RAM	JTAG	Field Conversion?
Yes		0	XNF	-	No	Yes
Yes		0	HDL	-	No	Yes
Yes		0	EDIF	-	No	Yes
	Yes	0	HDL	No	No	Yes
	Yes	0	XNF	No	No	Yes
	Yes	0	EDIF	No	No	Yes
Yes		7	HDL	-	No	Yes
Yes		7	XNF	-	No	Yes
Yes		7	EDIF	-	No	Yes

5200	4000/Spartan	Mode	Source	RAM	JTAG	Field Conversion?
	Yes	7	HDL	No	No	Yes
	Yes	7	XNF	No	No	Yes
	Yes	7	EDIF	No	No	Yes
	Yes	0	HDL	Yes	No	Yes
	Yes	7	HDL	Yes	No	Yes
	Yes	0 or 7	XNF	Yes	No	Yes
	Yes	0 or 7	EDIF	Yes	No	No
	Yes	0 or 7	Any	Yes	Yes	No

The complete conversion process and three source file dependent flows are outlined in Figure 1.

Figure 1. Xilinx Conversion Process



Notes:
1. Custom Boundary Scan logic for JTAG support is designed at the factory.
2. Figaro may reject some Xilinx-specific library components preserved during an XNF to EDIF conversion; refer to techref.pdf.
3. Check the package of the configurator and FPGA are available from Atmel.

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